**INTERNAL PRODUCT SPECIFICATION (IPS)**

MODEL NUMBER：

PRODUCT NAME: 7S1P Spider2 24V Battery Pack

CUSTOMER： Smith & Nephew

REFERENCE：

Inventus Power P/N: 902-09823-001

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Product PN | With heater or not | 15V AUX power | Operate mode | Communication | Remake | Mechanical |
| 902-09823-001 | No |  |  | SMBus |  |  |

THIS SPECIFICATION COVERS THE PERFORMANCE CHARACTERISTICS AND PRODUCTION TEST REQUIREMENT FOR

902-09823-001 7S1P Smith & Nephew Spider2 24V Battery Pack

Contents

[**Revision History** 3](#_Toc149220130)

[**Product information Version List** 3](#_Toc149220131)

[1 SCOPE 6](#_Toc149220132)

[2 GENERAL REQUIREMENTS 6](#_Toc149220133)

[3 ELECTRICAL SPECIFICATION 6](#_Toc149220134)

[4 MATERIAL AND CONSTRUCTION REQUIREMENTS 7](#_Toc149220135)

[5 PCBA SPECIFICATION 7](#_Toc149220136)

[5.1 Scope 7](#_Toc149220137)

[5.2 PCBA specification of Mainboard 7](#_Toc149220138)

[5.2.1 Scope 7](#_Toc149220139)

[5.2.2 General request 8](#_Toc149220140)

[5.2.3 Firmware information 8](#_Toc149220141)

[5.2.4 Electrical reference files 9](#_Toc149220142)

[5.2.5 Mechanical assemble require 10](#_Toc149220143)

[5.2.6 Label and package information 10](#_Toc149220144)

[5.2.7 PCBA Function test 10](#_Toc149220145)

[6 Unit specification 16](#_Toc149220146)

[6.1 Scope 16](#_Toc149220147)

[6.2 Unit specification for -001 projects 17](#_Toc149220148)

[6.2.1 Scope 17](#_Toc149220149)

[6.2.2 General request 17](#_Toc149220150)

[6.2.3 Firmware information 17](#_Toc149220151)

[6.2.4 Schematic files 17](#_Toc149220152)

[6.2.5 Mechanical Assembly and mechanical test Require 18](#_Toc149220153)

[6.2.6 Label and package information 25](#_Toc149220154)

[6.2.7 Unit function test 25](#_Toc149220155)

[7 QUALITY ASSURANCE REQUIREMENT 33](#_Toc149220156)

[7.1 QA Product Verification 33](#_Toc149220157)

[7.2 Incoming Quality Control (IQC) 33](#_Toc149220158)

[7.3 Testing 33](#_Toc149220159)

[7.4 QC Audit 34](#_Toc149220160)

**Revision History**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Revision** | **Reason of change** | **Change by** | **Check by** | **Date** |
| X1 | New release | Cisca | Kylin/CYW | 2025-05-14 |
| X2 | Update 6.2.7.2 burn in test | Cisca | Kylin/CYW | 2025-06-17 |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |

**Product information Version List**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Item | Designation | Project PN | Document Name | Version | Issue Date |
| 1 | Customer Specification |  |  |  |  |
| 2 | Production code |  |  |  |  |
|  |  |  |  |
| 3 | Programming tool |  |  | N/A |  |
| 4 | Calibrator |  |  |  |  |
| 5 | PCM tester software |  |  |  |  |
| 6 | Unit tester software |  |  |  |  |
| 7 | Cycle test software |  |  |  |  |
| 8 | PCB |  |  | N/A |  |
| 9 | Schematic |  |  | N/A |  |
| 10 | Assembling Drawing |  |  |  |  |
| 11 | Assembling flow chart |  |  |  |  |
|  |
| 12 | PCBA Label |  |  | N/A |  |
|  |
| 13 | Unit Label |  |  | N/A |  |
|  |
| 14 | Inner box label |  |  | N/A |  |
|  |
| 15 | Outer box label 1 |  |  | N/A |  |
|  |
| 16 | Outer box label 2 |  |  | N/A |  |
|  |
| 17 | Traceability |  |  | N/A |  |

# SCOPE

This specification defines the performance characteristics and production test requirement for 7S1P Smith & Nephew Spider2 24V Battery pack

# GENERAL REQUIREMENTS

This specification describes the requirements for the rechargeable Lithium-ion battery pack. This battery pack is designed with integral electronic circuit providing cell protection, fuel gauge required.

# ELECTRICAL SPECIFICATION

1. Over-Charge Protection Voltage: 4.15 ± 0.015 V / Cell
2. Over-Charge Release Voltage: 3.6± 0.015 V / Cell
3. Over-Discharge Protection Voltage: 2.70 ± 0.015 V / Cell
4. Over-Discharge Release Voltage: 3.30 ± 0.015 V / Cell
5. Over-Charge Current Protection: 2.5A ± 0.3A 10S
6. Over-Discharge Current Protection: 5A ±0.5A 30s
7. Charge Over-Temperature Protection: 55°C ± 3°C
8. Charge Over-Temperature Release: 50℃ ± 3°C
9. Discharge Over-Temperature Protection: 70℃ ± 3°C
10. Discharge Over-Temperature Release: 65℃ ± 3°C
11. Pack AC Impendence: TBD
12. Electro-Static discharge (ESD): ± 8 KV (Contact), ± 15 KV (Air)
13. Leak current:  300~700 uA (sleep mode)

10~20 uA (shutdown mode)

# MATERIAL AND CONSTRUCTION REQUIREMENTS

Material and construction shall be exactly as specified by engineering document, BOM and mechanical drawing. No deviation is permitted without written authorization from engineering. Materials are chosen such that the performance and product specification specified herein will be met when the battery pack is subject to the specified environment conditions.

# PCBA SPECIFICATION

## Scope

This specification specifies the specification for all the PCBAs using at 9823 projects.

And it will apply to below PCBA:

201-0007913 Main board

## PCBA specification of Mainboard

### Scope

This specification specifies the standard request, firmware information, schematic file, PCB Gerber file, material and construction, mechanical requirement/test, label and package information, package test, PCBA function test of the PCBA.

And it will apply to below PCBAs:

201-0007913

### General request

#### AOI test requirement:

To inspect the mounting and the soldering quality, inspect 100% of the assemblies via an AOI (automatic optical inspection). The components which will not be covered in ICT test must be specially well monitored in AOL process.

Especially for below components

### Firmware information

### Electrical reference files

|  |  |
| --- | --- |
|  | 201-0007944 |
| Schematic | Refer to official release |
| PCB Gerber file | Refer to official release |
| PCB  E-drawing | Refer to official release |
| Silkscreen | Refer to official release |
| Pick and placement | Refer to official release |
| PCB Fabrication Requirement | Refer to official release |

### Mechanical assemble require

### Label and package information

### PCBA Function test

#### Required test condition and equipment

1) All tests must be conducted in the 25℃±5℃ AMT environment.

2) Equipment Reference List

|  |  |  |
| --- | --- | --- |
| Equipment | Requirement | Quality |
| DC | 40V, 30A | 2 |
| E-load | 4000W | 2 |
| Multi-Meter | --- | 6 |
| Variable-Resistance Box | 0~100K | 0 |
| PC | --- | 1 |
| USBCANEU | --- | 1 |

#### Test Diagram

All tests must be conducted in the typical 25℃±3℃ AMT environment

Equipment:

DC1：60V/10A power supply; DC2: 60V/12A power supply; E-load1:60V/1000W; E-load2:60V/1000W.

Add 68V TVS18 (M5558-008) between cell positive and negative

Add 5V TVS as below (TVS1~TVS16), the part number of TVS is Panjit#SA5.0A

Note: All 5V TVS should close to daughter board as possible, it should be mounted on the test pin, not on dummy battery pack board

图示, 示意图

AI 生成的内容可能不正确。



Diagram4-1

#### Test item and procedure

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test items  &  Apply to project PN | **Test Content** | **Test method & condition** | **Test result (Spec)** | Remark |
|  | **Three terminal fuses 1** | 1. Connect the PCBA as Diagram4-1 2. Short J5 and close SW3,SW5(Keep the status until all test over.) 3. Test TP52 and TP55. The resistance less than 1 ohm. 4. Test the resister between TP34 and TP47 5. Test the resister between TP35 and TP47 6. The resister rang should be 20.8~31.2 ohm. | **Pass/ fail** | Refer to Diagram4-1 |
|  | **Reference voltage test** | 1. Connect the PCBA as Diagram4-1 2. Turn on SW4，SW1 3. Set E-load1 to CV 25.2V@5A 4. Set DC1 to 30V@1A. 5. Set DC2 to 25.2V@1A, 6. Turn on E-load1, DC1 then turn on DC2 then turn DC2 off. 7. Wait about 1s, check communication with PC 8. Test bellow basic voltage.  |  |  |  | | --- | --- | --- | | Quantity to be measured | Measured at point | Reference point | | +15V | TA64 | T87 | | +3.3V | TP3 | T87 | | 3.3V=3.3V+/-0.2V  15V=15V+/-0.5V | Refer to Diagram4-1 |
|  | **Cell voltage and current calibration** | 1. Connect SMbus communication to PC 2. Set DC1=30V@1A Eload1 CV 25.2V 3. DC2 =25.2V@0.1A 4. Turn on DC1,Eload1 5. Turn on DC2, after 2s turn off 6. Record offset voltage between PCBA and multimeter: (Cell voltage SMBus commands: Cell1 0x3c; Cell2 0x3d; Cell3 0x3e; Cell4 0x3f; Cell5 0x40; Cell6 0x41; Cell7 0x42; Cell8 0x43;) 7. △VCell1=Vcell1-VSMbus\_cell1<±5mV 8. △VCell2=Vcell2-VSMbus\_cell2<±5mV 9. △VCell3=Vcell3-VSMbus\_cell3<±5mV 10. △VCell4=Vcell4-VSMbus\_cell4<±5mV 11. △VCell5=Vcell5-VSMbus\_cell5<±5mV 12. △VCell6=Vcell6-VSMbus\_cell6<±5mV 13. △VCell7=Vcell7-VSMbus\_cell7<±5mV 14. △Current\_0A= ISMbus\_current<±10mA 15. Set E-load2 CC 5A 16. Turn on E-load2(current command: 0x0a) 17. △Current\_5A=Actual current - ISMbus\_current <±100mA | offset voltage between multimeter and PCBA:  1, △VCell < ±5mV;  2, △Current\_0A <±10mA | Refer to Diagram4-1 |
|  | **Batt voltage tolerance** | 1. Read the Batt voltage by SMBus 2. Record voltage of V2 3. The voltage different between SMBus and multi meter is ±0.5V . | Batt voltage: tolerance: ±0.5V | Refer to Diagram4-1 |
|  | **Charge current verify and test** | 1. Set E-load1 to CV25.2V@10A 2. Set DC1 to 30V@1A 3. Set DC2 to 28V@0.9A 4. Turn on SW1, SW4 5. Reduce DC2 to 22V 6. Test charge current on RS1 TP85 and TP86, read the 0A charge current by A2, and read by SMBus at the same time, compare the difference. 7. Increase DC2 to28.7V 8. Test charge current, read the 0.9A charge current by A2, and read by SMBus at the same time, compare the difference | RS1 charge current tolerance:  +0.9A:  <+/-20mA | Refer to Diagram4-1 |
|  | **Discharge current verify** | 1. Set E-load1 to CV25.2V@10A. 2. Set DC1 to 30V@5A. 3. Close SW1 to wake up pack. 4. After 3S, the pack can discharge normal. V1=25.2V±1V 5. Set E-load2 to CC 4 A. 6. Close SW2 7. Read the 4A discharge current by SMBus and compare with A2 test data. 8. Record current of A2 | RS1 discharge current tolerance:  +4A:  <+/-0.04A |  |
|  | **Temperature** **tolerance** | 1. Read the Cell temperature, Pack temperature and MOSFET temperature by SMBus. 2. Record the temperature of ambient. 3. Compare the temperature different between SMBus and ambient is +/-3℃.. | Cell temperature +/-10℃.(Cell\_NTC1,2)  PCBA connector (NTC3,4) and MOSFET temperature (NTC5)+/-10℃. | Refer to Diagram4-1 |
|  | **DCR of PCBA** | 1. Keep the state of 5.2.7.3.7 2. Record voltageV1 and V2 3. DCR=(V1-V2)/A2 | DCR value:  7.2±2mOHM | Refer to Diagram4-1 |
|  | **UVP test** | 1. Connect the PCBA as Diagram4-1 2. Turn on SW2, SW4 3. Set E-load1 to CV 24@5A 4. Set DC1 to 30V@2A. 5. Set DC2 to 25.2V@2A, 6. Turn on E-load1, DC1, DC2.and turn off DC2 7. Set E-load2 to be CC 1A 8. Turn on E-load2 9. Sent Command to check DSG MOSFET can be turn off or not 10. Turn off E-load2 and wait the PCBA recover and star discharge again 11. Turn on E-Load2 12. Gradually decrease E-load1 voltage by step(100mV@4s/time), record multi meter V1 and V3 voltage when current or A2 change to be 0A from 1A. 13. The voltage is over-discharge voltage. | Turn off DSGMOSFET:  Pass/fail  UVP value:  V1:19.14±0.2V  V3: 2.732V±0.05V  (No need to test in PP) | Refer to Diagram4-1  (Only test max. limit and min. limit to judge PASS/FAIL in PP and MP) |
|  | **Full charge & OVP test** | 1. Connect the PCBA as Diagram4-1 2. Turn on SW1,SW4 3. Set E-load1 to CV 27V@5A 4. Set DC1 to 32V@0.1A. 5. Set DC2 to 28V@1A, 6. Turn on E-load1, DC1, DC2. 7. Then A2=1A±5% 8. Sent Command to check CHG MOSFET can be turn off or not 9. Turn off DC2 and wait the PCBA recover and star charge again 10. Gradually increase E-load1 voltage by step (100mV@4s/time), record multi meter V1 voltage when current A2 change to be 0A from 1A. 11. The voltage is full-charge voltage. 12. Then continue increase E-load1 voltage until over charge protect flat bit show, record the OVP voltage | Turn OFF CHGMOSFET:  pass/fail  Full charge value:  28.7V±0.2V  OVP value:  29.05V±0.2V  (No need to test in PP) | Refer to Diagram4-1  (Only test max. limit and min. limit to judge PASS/FAIL in PP and MP) |
|  | **2nd OVP test** | 1. Connect the PCBA as Diagram4-1 2. Turn on SW1, SW4 3. Set E-load1 to CV 28V@5A 4. Set DC1 to 32V@0.1A. 5. Set DC2 to 32V@1A, 6. Turn on E-load1, DC1,DC2 7. Test the voltage of TP6 record as A, A should < 1V 8. Turn off SW3 9. Increase Cell1 voltage until the voltage of TP6 = B(4~14V) 10. Record the cell1 voltage as C 11. Reduce the voltage of cell1 to 3V, test the voltage of TP6, record as A, A should < 1V 12. Turn on SW3 and turn off SW5 13. Increase Cell6 voltage until the voltage of TP6 = B(4~14.7V) 14. Record the cell6 voltage as D | C, D, = 4.25V +/- 25mV | Refer to Diagram4-1  (Only test max. limit and min. limit to judge PASS/FAIL in PP and MP) |
|  | **Sleep mode and shut down mode standby current test** | 1. Connect the PCBA as Diagram4-1 2. Turn on SW1, SW4 3. Set E-load1 to CV 24V@5A 4. Set DC1 to 29V@0.1A. 5. Set DC2 to 25V@2A, 6. Turn on E-load1,DC1,DC2 7. Turn off DC2 Active the battery 8. Physicals disconnect all communication, DC2, SW1 9. Wait about 3min (or sent command) to enter Sleep mode 10. Test TP44 voltage should 24V±1V 11. Record the A1 current as A 12. Turn on DC2 Active the battery 13. Reduce the E-load1 to CV 17.5V 14. Wait about 60S (or sent command”0 10”, if using command, you can skip step) to enter shutdown mode 15. Test TP44 voltage should less than 1V 16. Record the A1 current as B | Shutdown mode current:  A = 10uA±2uA  Sleep mode current:  B = 1mA±0.2mA | Refer to Diagram4-1 |

# Unit specification

## Scope

This specification specifies the specification for all the units using at 9823 project.

And it will apply to below products:

903-09823-001

## Unit specification for -001 projects

### Scope

This specification specifies the standard request, firmware information, schematic file, material and construction, mechanical requirement/test, label and package information, package test, Unit function test of the Unit.

Apply to below project PN:

902-09823-001

### General request

Need inspect below items:

Inspect 100% of short/open circuit for the connectors soldering.

Inspect if the nickel sheet connected well

Inspect if all the assembly materials are assembly or not

Inspect if some defect at the housing.

### Firmware information

### Schematic files

|  |  |  |
| --- | --- | --- |
|  | 902-09823-001 |  |
| PCBA PN | Main: 201-0007913  LED: 201-0007944 |  |
| Schematic | Main: 301-000784-001  LED: 301-000788-001 |  |

### Mechanical Assembly and mechanical test Require

#### Glue added required

#### Screw torque force require

#### Mechanical Test

##### Vibration test

A screenshot of a test

Description automatically generated

##### Free fall test

A close-up of a battery

Description automatically generated

##### Mechanical shock (crash hazard)

A close-up of a test

Description automatically generated

### Label and package information

### Unit function test

#### Required test condition and equipment

1) All tests must be conducted in the 25℃±5‘C AMT environment.

2) Equipment Reference List

|  |  |  |
| --- | --- | --- |
| Equipment | Requirement | Quality |
| DC | 60V@ 30A  12V@1A | 1  1 |
| E-load | 60V @50A | 1 |
| Multi-Meter |  | 4 |
| Variable-Resistance Box |  |  |
| PC |  |  |
| EV2300 |  |  |
| power resistor | 100 ohm / 50W | 1 |
| capacitor | 15000uf / 100V | 1 |

#### Signal pin defined

#### Test item and procedure

Note: These unit function test should be done after the Hi-pot and burn-in test was complete.

**Cell matching**

Before assembling, all the 7 cells in one unit must be confirmed to have similar performance as below:

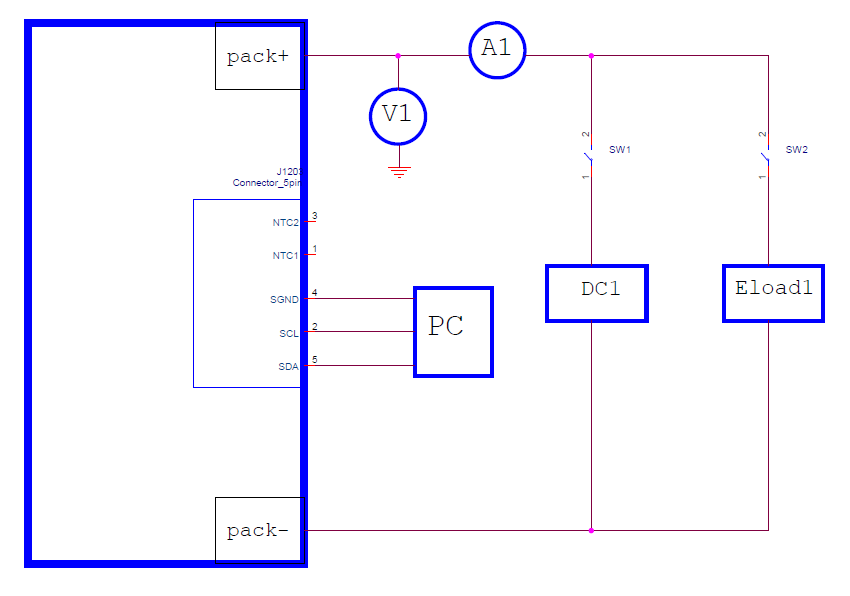
1. their difference of open circuit voltage must be less than 8mV

(Vcell\_max-Vcell\_mix<8mV)

1. The difference of impedance must be less than 3 milli ohm

(Rcell\_max-Cell\_min<=3m ohm)

1. All the cells must be picked from the same production lot/same date code recorded by cell manufacturer.
2. Below test can be apply to 9823-001



Unit Test Digram

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Unit Test** | | | | |
|  | **Current calibration** | Current calibrating point as below  0A±0.02A  3A±0.06A | Pass/Fail |  |
|  | **Burn-in test** | 1. Set DC1 28.7V 0.9A, 2. Turn on DC1, SW1, to charge the battery pack full 3. Then turn off DC1, SW1 4. Set the E-load1 CC 4.5A 5. Turn on E-load1, SW2 to discharge the battery pack until empty 6. Then turn off E-load1, SW2. 7. Turn on DC1, SW1 to charge the battery pack until SOC=20%~30%. 8. Record the Cell voltage, temperature, current information in the burn in test. 9. Test request: No fault occur, Differential of cell Voltage<20mV, Cell temp<45℃ | Pass/Fail | Refer  unit test diagram |
|  | **Charge current** | 1. Set DC1 to 28.7V 0.9A 2. Turn on SW1 3. Then the charge current should <0.1A 4. Turn on DC1 5. Read the charge current by SMBus, it should be 0.9A+/-0.02A | Current:  0.9A+/-0.02A | Refer  unit test diagram |
|  | **Pack voltage** | 1. Connect as Unit Test diagram 2. Read the Pack voltage by SMBus 3. Record voltage of V1 4. The voltage different between SMBus and multi meter is ±1V | Pack voltage tolerance of SMBus : ±1V | Refer  unit test diagram |
|  | **Cell voltage balancing test** | 1. Keep the status as latest test. 2. Read all Cell voltage by SMBus 3. Calculate V cell(max)-V cell(min) | V cell(max)- V cell(min)< 10mV. | Refer  unit test diagram |
|  | **Offset current test** | 1. No charge and no discharge   Read discharge current by SMBus | The offset current should=0±20mA. | Refer  unit test diagram |
|  | **4.5A discharge current tolerance** | Option 1   1. Set E-load1 to 4.5A 2. Turn on SW2 3. Turn on E-load1, and read the discharge current by SMBus 4. It should be 4.5A+/-0.06A | The current read by  Option 1  CAN bus should: 4.5A +/- 60mA | Refer  unit test diagram |
|  | **Temperature test** | 1. Read the Cell temperature and PCBA temperature and MOSFET temperature by SMBus 2. Record the temperature of ambient 3. Compare the temperature different between SMBus and ambient. 4. Record as A | Cell temperature:  A=+/-10℃(Cell\_NTC1-2)  temperature(NTC4, NTC5) and MOSFET temperature(NTC3):A=+/-10℃ | Refer  unit test diagram |
|  | **Battery pack internal impedance** | 1. Measure the battery pack voltage (no load) and record the voltage (Vo). 2. Set E-load1=CC1A 3. Turn on E-load1, after 3 seconds, record the battery pack output voltage(V2) 4. Turn of E-load1 5. Calculate impedance=(Vo-V2)/1A | Measure 50pcs-100pcs packs impedance at the same ambient temperature(±3℃). And draw the impedances distribution as Figure\_3.  When -3σ<μ<3σ, the pack impedance is positive.  When μ<-3σ orμ>3σ, please check this pack assembly craft(e.g. Cell touch welding impedance; Cell connect impedance; Pack connect impedance. Etc.). | Refer  unit test diagram |
|  | **CHG FET and DSG FET test** | 1. Sent command ”00 40””00 789A” to close CHG FET, charging should disable, and current should be 0        1. Sent command ”00 40””00 7899” to close DSG FET, discharging should disable, and current should be 0 | Pass or not | Refer  unit test diagram |
|  | **Write manufacturing Info** | (1) Write Manufacture Data   1. Base on below formula write the HXE value into battery pack by command 0x1B. 2. Formula :   (Year - 1980) \* 512 + Month \* 32 + day   1. Such as the day is 5/23/2017, the value is (2017-1980)\*512 + 05\*32 + 23 = 19127 0x4AB7, then at command 0x1B write value 0x4AB7 into battery pack.   (2) Write Serial Number   1. The Serial format is 0x0001~0xFFFF 2. According to the serial number of label. Write the HEX into battery pack for every battery by command 0x1C. |  |  |
|  | **Verify manufacturing Info** | (1) Verify Manufacture Data   1. Read command 0x1B, Compare, if the read back value is the same as the write value Pass Otherwise Fail   （2）Verify Serial Number  Read command 0x1C, Compare, if the read back value is the same as the write value Pass Otherwise Fail |  |  |
|  | **△OCV after 3days up to 10days** | **Before storage:**   1. Rest battery pack 2hour. 2. Read individual cell OCV value and pack OCV value from SMBus, record 8 data, Vcell1\_old ~ Vcell7\_old, V batt\_ old. 3. Compare individual cell OCV value from SMBus, the cell voltage difference shall be less than 20mV   （0≤V cell max\_ old-V cell min\_ old <10mV if the cell voltage difference > 10mV need to wait the battery pack to balance）   1. The difference of pack OCV value with total cell voltage shall be less than 250mV   (0≤V batt\_ old- Vcell1\_old -…-Vcell7\_old <±250mV)  Send a comment “0 10” to let the battery pack into shutdown mode    **After 5 days storage:**   1. Active the battery pack. 2. Read SMBus data after 5 days storage, record Vcell1\_new ~ Vcell7\_new, V batt\_ new. Totally 17datas. 3. Check the storage time, the storage time shall be 4320minutes. ~14400minutes 4. Compare individual cell OCV value from SMBus, the cell voltage difference shall be less than 20mV.   (0≤V cell max\_ new-V cell min\_ new<20mV）   1. The difference of pack OCV value with total cell voltage shall be less than 250mV. (0≤V batt\_ new – Vcell1\_new -…-Vcell7\_new< ±250mV)   **5 days storage compare:**   1. Compare “New” and “Old” individual cell OCV data of each cell, the difference shall be less than 4mV\*N(days).   (0≤Vcell1\_old-Vcell1\_new<4mV\*N(days)  …  Vcell7\_old-Vcell7\_new<4mV\*N(days))   1. Compare New and Old OCV data of pack, (0≤V batt\_ old – V batt\_ new**<**50mV\*N(days). 2. Find out the min OCV cell and compare its OCV with 3-10days ago. | Read the pack OCV from SMBus , should be within 24.15V~ 24.85V and record SOC | Refer  unit test diagram |
|  | **Shipment OCV and SOC FCC** | 1. Read SMBus”XXX”, SOC; 2. Read SMBus”XXXX”, FCC | 1. Record SOC and FCC 2. OCV: 24.15V~ 24.85V | Refer  unit test diagram |
|  | **Ship mode** | 1. Read the SOC from SMbus (20%-30%) 2. Send a comment “0 10”to let the battery pack into shutdown mode 3. Test the output voltage | Output voltage<=1V | Refer  unit test diagram |

# QUALITY ASSURANCE REQUIREMENT

## QA Product Verification

Detail inspections, functional test, environmental test and reliability test will be carried out at both design and manufacturing stages. The procedure is in line with product quality plan.

## Incoming Quality Control (IQC)

Sample will be drawn from every lot delivered according to the ANSI/ASQC Z1.4 procedure followed is per the F.I.L. incoming material review board flow chart. The inspection criteria will be in line with the F.I.L. engineering sample approval report (SER) and drawing.

## Testing

Testing will be carried out at initial and final test station to guarantee that every unit leaving the factory will meet the requirement in section 5.

## QC Audit

All units, which are pass QC final test and packaging will be randomly sampled by QC audit team. Lot size will depend on standard ANSI/ASQC Z1.4.

*PRE-SHIPMENT AUDIT - LEVEL S3*

*OUTGOING - LEVEL II*

**1).** SAMPLING TO CHECK Capacitance OF BATTERY PACK --- 60AH MIN FOR EACHE LOT; THE TEST CONDITION AS FOLLOW:

STANDARD CHARGING: CC 20A UNTIL THE PACK ATUO PROTECTION

STANDARD DISCHARGING: CC 120A UNTIL THE PACK ATUO ROTECTION

**2).** SAMPING TO CHECK THE SELF-DISCHARGE VOLTAGE DROP FOR EACH LOT, THE AVERAGE VALUE SHOULD BE 10mV/ PER DAY.(redefine base on PP data)